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User Guide Abstract This document is for the person who installs, administers, and troubleshoots servers and storage systems. Hewlett Packard Enterprise assumes you are qualified in the servicing of computer equipment and trained in recognizing hazards in products with hazardous energy levels. Part Number: 775786-004 March 2016 Edition: 4

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1. Navigate to ./software/user/example under the design example directory. 2. Compile the design example application: \$ make 3. Run the test: \$./intel_fpga_pcie_link_test You can run the Intel FPGA IP PCIe link test in manual or automatic mode. — In automatic mode, the application automatically selects the device. The test

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Arria 10 Hard IP for PCI Express User Guide for the Avalon Memory-Mapped Interface Last updated for Altera Complete Design Suite: 13.1 Arria 10 101 Innovation Drive San Jose, CA 95134 www.altera.com UG-01145_avmm December2013 Subscribe Send Feedback

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Intel Stratix® 10 FPGAs include a configurable, hardened protocol stack for PCI Express® that is compliant with PCI Express Base Specification 3.0. The Stratix 10 Hard IP for PCI Express IP Core supports Gen1, Gen2 and Gen3 data rates and x1, x2, x4, x8, or x16 configurations. Figure 1. Stratix 10 PCIe Variant with Avalon-ST Interface

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Installing a full-length mini-PCIe module Procedure 1. Align the full-length mini-PCIe module with the full-length slot on the mini-PCIe adapter board. 2. Insert the mini-PCIe module connector into the slot. 3. Using a Phillips screwdriver, insert and tighten the two screws to secure the mini-PCIe module to the board. Page 33: Configuration

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